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#### Article

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# A Fast Extraction Method of Energy Distribution of Border Traps in AlGa<sub>N</sub>/Ga<sub>N</sub> MIS-HEMT

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**ABSTRACT** MIS-HEMT is one of the most promising structures to prohibit the unfavorable gate leakage in conventional AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs. However, the extra insulator layer introduces massive border traps at insulator/AlGa<sub>N</sub> interface and results in the poor reliability. In this brief the energy distribution of border traps in AlGa<sub>N</sub>/Ga<sub>N</sub> MIS-HEMT gate stack is extracted and investigated through a discharging-based trap energy profile technique. The technique adopts spot- $I_d$  sense measurement with 1 millisecond measurement time to capture the “whole (both fast and slow)” border traps. The results are beneficial to improve the reliability of AlGa<sub>N</sub>/Ga<sub>N</sub> MIS-HEMT.

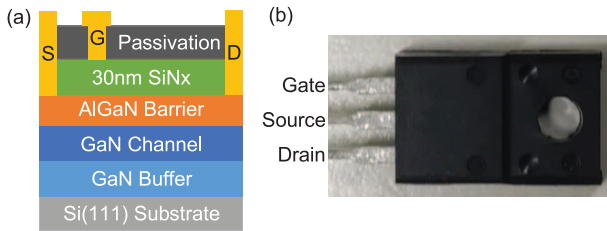
**INDEX TERMS** Ga<sub>N</sub> MIS-HEMT, energy distribution.

## I. INTRODUCTION

Owing to the large bandgap, high breakdown electric field and high saturation electron mobility, Ga<sub>N</sub> has been considered as one of the most promising candidates to replace silicon, which is now approaching its physical limitation, in power electric applications. The past 3 decades witness the booming development of Ga<sub>N</sub>-based high electron mobility transistors (HEMTs). Conventional AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs usually suffer from the high-gate leakage, resulting in an unfavorable power loss during an OFF-state condition and a low-gate overdrive during ON-state condition. MIS-HEMT structure needs to be adopted to suppress the gate leakage. However, due to the existence of vast number of traps in the gate stack, the reliability of AlGa<sub>N</sub>/Ga<sub>N</sub> MIS-HEMTs becomes one of the major concerns and precludes their commercial applications.

To improve the performance and reliability of Ga<sub>N</sub>-based MIS-HEMT, energy distribution of the border traps at insulator/AlGa<sub>N</sub> interface need to be investigated.

Among the traditional characterization techniques on Ga<sub>N</sub>-based HEMTs, photo-assisted techniques such as Electroluminescence (EL) characterization [1], [2] and photoionization spectroscopy [3], [4] need to heavily stress the device and will generate new traps during the measurement, thus cannot be adopted to investigate the border traps' energy distribution. Deep level transient spectroscopy (DLTS) [5], [6] mainly characterizes the deep level traps as the name suggests and the test samples need to go through repetitive CV measurements under various temperatures from cryogenic temperature to high temperature, which might also create new traps. Low frequency noise technique could probe the overall trap density [7]–[9], but the technique relies on the assumption of uniform distribution of traps in area, depth, and energy [10]. Tallarico *et al.* [11] proposed a spatial and energy distribution extraction technique of traps in p-channel of power U-MOSFETs, but the traps were characterized through slow DC I/V sweep measurements which cannot probe fast recoverable traps.



**FIGURE 1.** Device structure: (a) The schematic diagram of cross section and (b) photograph of the TO-247 packaged device.

To the author's knowledge, the energy distribution of the border traps in AlGaIn/GaN MIS-HEMT gate stack across the entire energy range has not been widely studied yet.

We have recently developed a threshold voltage shift ( $\Delta V_{th}$ ) based technique that can probe the energy distribution of positive charges across the whole energy domain for Si MOSFETs using fast pulse measurements [12]–[15]. Similar methodology is adopted in this work for AlGaIn/GaN MIS-HEMT. Due to the power limitation of the commercial pulse measurement units, their output voltage range is usually insufficient for power devices. To make the technique more universal and applicable on mainstream semiconductor analyzer equipment such as source measure units (SMUs), a discharging-based trap energy profile (DTEP) technique is proposed in this work to overcome this output voltage range issue by replacing the fast pulse measurements with DC spot- $I_d$  measurements, as detailed in Section II.

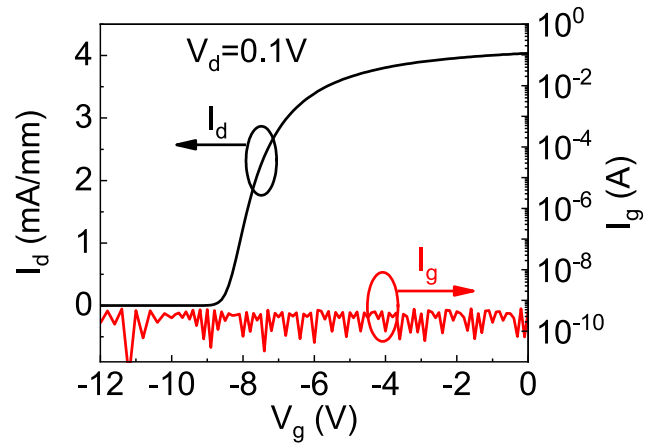
## II. DEVICE PREPARATION

The structure of the AlGaIn/GaN MIS-HEMT device used in this work is given in Fig. 1.  $Al_{0.25}Ga_{0.75}N/GaN$  heterostructure was grown on Si (111) substrate, which consists of a 25 nm  $Al_{0.25}Ga_{0.75}N$  barrier layer, a 2  $\mu m$  GaN buffer layer, and a GaN transition layer. A 30 nm  $SiN_x$  layer was then deposited on the AlGaIn barrier layer for dielectric layer. The device has a gate length of 4  $\mu m$ , a gate width of 17 mm, gate-source space of 3  $\mu m$ , and gate-drain space of 15  $\mu m$ . Finally, the  $SiO_2/SiN_x$  (300 nm/600 nm) was grown on the surface to passivate device. Owing to the high energy barrier of  $SiN_x$  layer, the gate leakage is suppressed to sub 1nA across the entire operation region, as shown in Fig. 2.

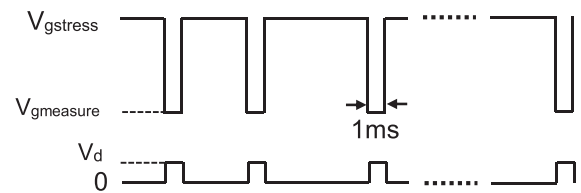
## III. EXPERIMENTS AND RESULTS

### A. CHARACTERIZATION OF DEGRADATION UNDER FORWARD AND REVERSE BIAS STRESS

To suppress the unintentional recovery during the measurement, spot- $I_d$  [16] sense measurement is adopted instead of slow DC I/V sweep measurement to characterize the degradation as shown in Fig. 3. Prior to the stress, a pre-stress DC I–V sweep with  $V_g$  sweeps from  $-10V$  to  $0V$  and  $V_d = 0.1V$  is performed with the device (not drawn in Fig. 3) and serves as reference characteristic for the determination of the threshold voltage shift ( $\Delta V_{th}$ ). A stress voltage,  $V_{gstress}$ , is then applied on the device, an intermittent drain current  $I_d$  sensing at  $V_{gmeasure}$  is monitored in



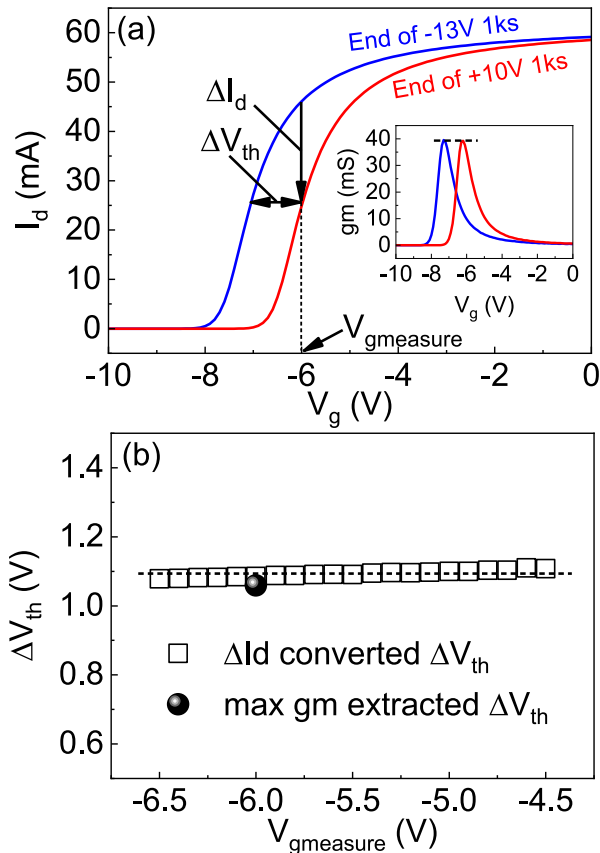
**FIGURE 2.** Transfer characteristic and gate leakage of the device,  $V_d = 0.1V$ .



**FIGURE 3.** Test waveform of the spot- $I_d$  sense measurement.

a preset log-incremental stress time to capture the degradation kinetics. Drain is biased at 0V during stress phase and 0.1V during sense phase. Measurement time is set to 1 millisecond as a trade-off between the gate lag effect [17] and the escaping of the fast recoverable border traps [18]. All the measurements are conducted on Keysight B1500A under room temperature (25°C). Note due to the limitation of Keysight B1500 software [19], the waveform in Fig. 3 needs to be constructed by a combination of multiple I/V-t sampling tests, and there is a  $\sim 2$  seconds delay between 2 different tests, users need to switch on the “output bias hold” option to maintain the stress bias during the test delay, thus the stress time period cannot be set to less than 2 seconds. In this work, the minimum stress time was set to 5 seconds.

The spot- $I_d$  sense measurement converts the  $I_d$  drop ( $\Delta I_d$ ) at a constant  $V_{gmeasure}$  to  $\Delta V_{th}$  by projecting  $\Delta I_d$  to the fresh transfer characteristic, as shown in Fig. 4a. Note this conversion method is only accurate while the mobility and on-resistance remains unchanged before and after stress, which is the case on our device. Fig. 4 depicts a comparison between the transfer characteristics at the end of  $-13V$  1000s (1ks) and  $+10V$  1ks, it turns out the mobility and  $R_{on}$  do hardly changes in these 2 extreme cases, as shown in the inset of Fig. 4a, the max-gm value is the same for the two transfer characteristics, suggesting they possess the same mobility [20] and  $R_{on}$ . In addition,  $\Delta V_{th}$  at different  $V_{gmeasure}$  were calculated and compared with the max gm method extracted value, as shown in Fig. 4b. It is observed that  $V_{gmeasure}$  selection has little impact on  $\Delta V_{th}$  conversion,



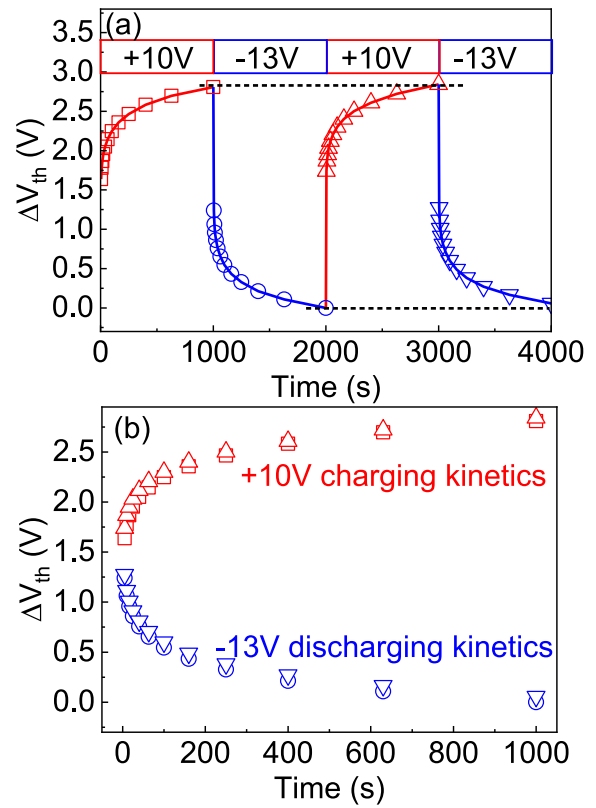
**FIGURE 4.** (a) Illustration of the  $\Delta I_d \sim \Delta V_{th}$  conversion, the 2 transfer characteristics were measured at the end of  $-13V$  1ks (blue) and  $+10V$  1ks (red), respectively. The inset shows the gm value of the 2 transfer characteristics. (b) Comparison of  $\Delta V_{th}$  converted from  $\Delta I_d$  at different  $V_{gmeasure}$  and extracted from max gm method.

and the converted  $\Delta V_{th}$  is very close to the max gm method extracted value, further justifying the spot-Id sense method.

A typical spot-Id sense experiment results are given in Fig. 5. The device is subjected to a  $+10V/-13V$  alternating stress, in each phase the stress time is set from 5s to 1ks. Fig. 5a shows  $\Delta V_{th}$  reaches 2.81V after  $+10V$  1ks stress, and the degradation can be fully recovered after  $-13V$  1ks. Note  $\Delta V_{th}$  here is much larger than the I/V sweep measurement (Fig. 4b), as it contains fast recoverable border traps. Moreover, the stress and recovery kinetics in different cycles exhibit tiny difference, as illustrated in Fig. 5b, indicating there is no trap generation during forward/reverse bias stress up/down to  $+10V/-13V$ .

## B. PRINCIPLES OF THE DTEP TECHNIQUE

The waveform of the proposed DTEP technique is depicted in Fig. 6. A spot Id sense measurement under high forward bias stress voltage,  $V_{gstress}$ , is firstly applied on the device to fill available border traps, stress time is set from 5s to 1ks. After the stress time reaches 1ks,  $V_g$  then steps down by a predefined  $\Delta V_g$  gradually to discharge the available border traps until the last  $V_{gdischarge}$  is met. The discharging



**FIGURE 5.** (a)  $\Delta V_{th}$  under  $+10V/-13V$  alternating forward/reverse bias stress, the  $+10V$  1ks stress induced degradation is fully recoverable under  $-13V$  1ks; (b)  $+10V/-13V$  exhibits the same charging/discharging kinetics, suggesting no extra traps were generated during forward/reverse bias stress.

time for each  $V_{gdischarge}$  is set from 5 seconds to 100 seconds to alleviating the charging effect under relatively high  $V_{gdischarge}$  levels, as detailed in the explanation of principles of the DTEP technique.

Fig. 7 illustrates the principles of DTEP technique to extract border traps' energy distribution. Considering the case of  $V_{gdischarge}$  drops from  $V_{gdischarge,i}$  to  $V_{gdischarge,i+1}$ , the fermi level  $E_f$  lowers down, accommodating a shaded region, where the filled border traps' energy is now above  $E_f$ . Given sufficient discharging time, all the border traps in the shaded region should be able to discharge, either by tunneling through the AlGaIn barrier or via trap-assisted conduction [21]. By sweeping  $V_{gdischarge}$  from the forwards bias stress level to the reverse bias, the density of border traps across the entire energy domain is achieved.

## C. ENERGY DISTRIBUTION EXTRACTION

Note since the spatial distribution of border traps is not known, and traps located in AlGaIn barrier and AlGaIn/GaN interface could also induce  $\Delta V_{th}$ , the concept of effective trap density is used in this work similarly to the early works [22], [23]. Traps are assumed to be at the  $SiN_x/AlGaIn$  interface and the effective density is required to induce the same  $\Delta V_{th}$  as that by the real spatially distributed traps spreading in the whole gate stack.

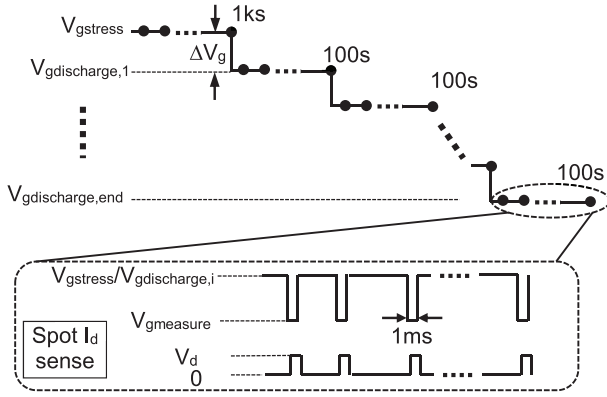
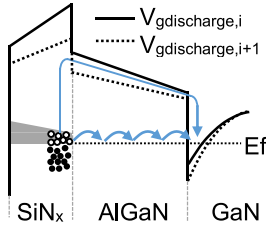
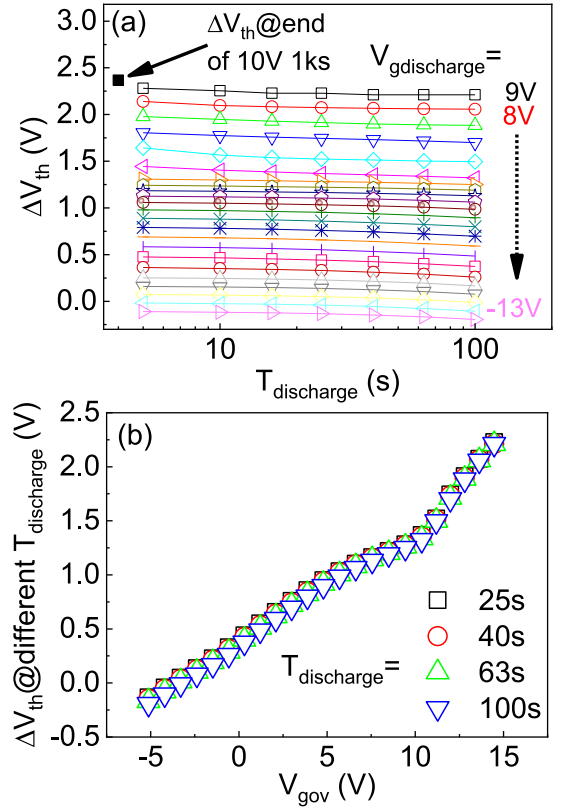


FIGURE 6. Test waveform of the DTEP technique.


 FIGURE 7. Illustration of the principle of DTEP technique to extract border traps' energy distribution, the solid/dashed band diagram represent the energy band under  $V_{gdischarge,i}/V_{gdischarge,i+1}$  respectively.

A typical test result of the DTEP technique is given in Fig. 8a.  $V_{gstress} = +10V$ ,  $V_{gdischarge}$  gradually lowers down from 9V to -13V at a constant step  $\Delta V_g = 1V$ . Note  $\Delta V_g$  cannot be set too small in order to guarantee discharging is dominant during all  $V_{gdischarge}$ . We see  $\Delta V_{th}$  reaches 2.37V after +10V 1ks stress.  $V_g$  then lowers down to  $V_{gdischarge,1} = 9V$ ,  $\Delta V_{th}$  starts to decrease due to the discharging of the border traps as explained before. As discharging time evolves,  $\Delta V_{th}$  gradually decreases, as shown by the '□' in Fig. 8a. Note since the first discharging time is already 5s, there is an abrupt drop of  $\Delta V_{th}$  from the last value of  $V_{gdischarge,i}$  to the first value of  $V_{gdischarge,i+1}$ , and suggesting the majority of border traps locate close to the  $SiN_x/AlGaIn$  interface and discharge within 5 seconds. After the discharging time  $T_{discharge}$  reaches the predefined value (100 seconds here to avoid further trapping and guarantee the discharging process to be dominant),  $V_{gdischarge}$  then keeps dropping and similar  $\Delta V_{th}$  kinetics against  $T_{discharge}$  is observed. By plotting the  $\Delta V_{th}$  value in the end of the discharging time against the corresponding overdrive voltage  $V_{gov} = V_g - V_{th}$ ,  $\Delta V_{th}$  profile against  $V_{gov}$  can be obtained, as shown by the '▽' in Fig. 8b. The  $\Delta V_{th} \sim V_{gov}$  profiles extracted at different discharging time are also plotted as a comparison in Fig. 8b, the negligible difference further indicates that 25~100 seconds is capable to discharge most available border traps.

To obtain the border traps' energy distribution,  $\Delta V_{th} \sim V_{gov}$  needs to be converted to trap density against trap energy. As we use effective trap density at  $SiN_x/AlGaIn$


 FIGURE 8. (a) Typical results of the DTEP technique. The slow down of  $\Delta V_{th}$  decline after 25s indicates the majority of available border traps are discharged. (b)  $\Delta V_{th}$  against  $V_{gov}$  at different  $T_{discharge}$ .

interface, the cumulative trap density  $N_{trap}$  can be obtained by

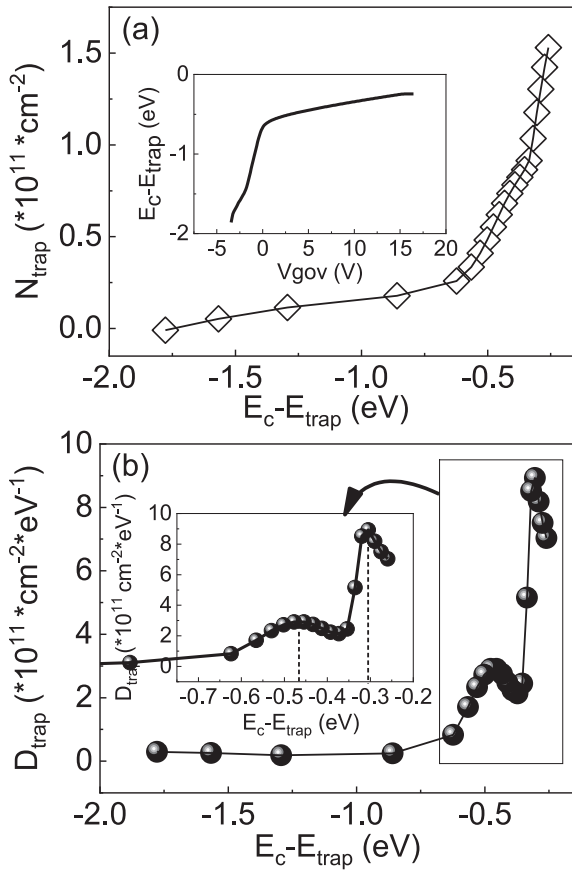
$$N_{trap} = \Delta V_{th} \cdot C_{SiN_x} / q \quad (1)$$

where  $q$  is the basic electric charge and  $C_{SiN_x}$  is the capacitance perunit area calculated by

$$C_{SiN_x} = \epsilon_{SiN_x} \cdot \epsilon_0 / T_{SiN_x} \quad (2)$$

where  $\epsilon_{SiN_x}$  is the coefficient of  $SiN_x$ ,  $\epsilon_0$  is vacuum dielectric constant and  $T_{SiN_x}$  is the thickness of the  $SiN_x$  dielectric layer. Assuming all the border traps above  $E_f$  is empty and below  $E_f$  is filled, the trap energy then equals to  $E_f$  thus its relation to  $V_{gov}$  can be obtained from TCAD simulations [24], as shown in the inset of Fig. 9a. Combining Equations 1&2 and  $V_{gov} \sim E_c - E_{trap}$  ( $E_c$  is the bottom of conduction band at  $SiN_x/AlGaIn$  interface), the cumulative trap density  $N_{trap} \sim E_c - E_{trap}$  distribution is calculated and shown in Fig. 9a. After obtaining  $N_{trap}$  distribution, density distribution  $D_{trap}$  can be derived from the first order differentiation on  $N_{trap}$ , as shown in Fig. 9b. Overall, in the range of  $E_c - E_{trap}$  from -1.78eV to -0.26eV,  $D_{trap}$  becomes higher as  $E_{trap}$  approaching  $E_c$ . Moreover, two notable peaks are observed at  $E_c - E_{trap} = -0.46eV$  and  $-0.3eV$ , with the peak density of  $2.91 \times 10^{11}$  and  $8.93 \times 10^{11} cm^{-2} \cdot eV^{-1}$  respectively.



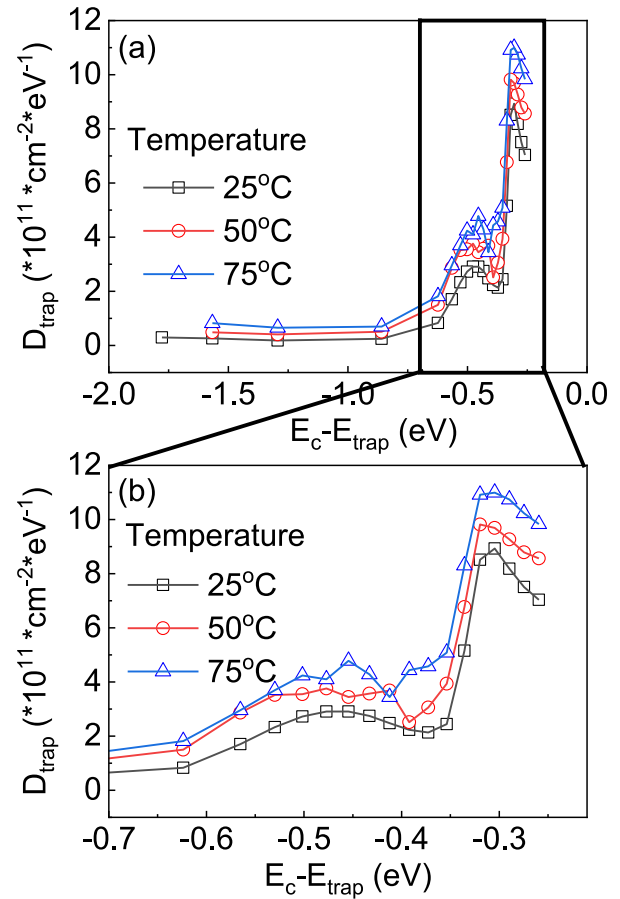


**FIGURE 9.** (a) Cumulative border traps' density  $N_{\text{trap}}$  against trap energy  $E_c - E_{\text{trap}}$ , the inset shows the conversion from  $V_{\text{gov}}$  to energy, which is obtained from TCAD simulation. (b) Energy distribution of border traps' density  $D_{\text{trap}}$  against trap energy  $E_c - E_{\text{trap}}$ , the inset enlarges the distribution plot in trap energy of  $[-0.75, -0.2]$  region for better observation.

To test the robustness of the proposed technique, DTEP experiments are conducted under different temperatures. The extracted energy distribution results are shown in Fig. 10. We see although the overall trap density distribution becomes slightly higher as temperature rises, they exhibit the same shape, indicating the extracted energy distribution is of physical meaning and the proposed technique is robust against temperature. The overall slight higher trap density might be caused by the fact that, some inactive traps under room temperature, either due to a further location from  $\text{SiN}_x/\text{AlGaIn}$  interface, or due to a high activation energy, become available to be involved (trapping/detrapping) within our experiment time domain under elevated temperatures.

#### IV. CONCLUSION

A discharging-based fast extraction method of energy distribution of border traps in AlGaIn/GaN MIS-HEMT is proposed in this brief. The method adopts spot- $I_d$  sense measurement with 1 millisecond measurement time to capture both fast and slow border traps. The experiment results show the overall border trap density,  $D_{\text{trap}}$ , becomes higher as  $E_{\text{trap}}$  approaching  $E_c$ , in the range of  $E_c - E_{\text{trap}}$  from -1.78 eV



**FIGURE 10.** (a) Effect of temperature on the energy distribution of  $D_{\text{trap}}$ . (b) An enlarged plot of  $D_{\text{trap}}$  energy distribution in trap energy range of  $[-0.7, -0.2]$  for clearer observation.

to  $-0.26$  eV. Moreover, two notable peaks are observed at  $E_c - E_{\text{trap}} = -0.46$  eV and  $-0.3$  eV, with the peak density of  $2.91 \times 10^{11}$  and  $8.93 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$  respectively. The method is of potential use for quick process screening and improvement of device performance and reliability.

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